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DATA CONVERSION INTERFACE BOARD DETAILED DESIGN DOCUMENT

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GLOSSARY

AtoD:	*Analog to Digital* conversion
DCS:	*Data Conversion System*
DCIB:	*Data Conversion Interface Bus*
DFB:	*Differential Fast Bus,* used by the disk array
DSP:	*Digital Signal Processing*
EARS:	*Experimental Array Radar System*
FIFO:	*First-in, First-out memory*
IF:	*Intermediate Frequency*
I/O:	*Input/Output*
MB:	*Megabyte*
MHz:	*Megahertz*
MTU:	*Master Timing Unit*
PC:	*Personal Computer*
PRF:	*Pulse Repetition Frequency*
RF:	*Radio Frequency*
SCSI:	*Small Computer System Interface*
SRAM:	*Static Random Access Memory*
VME:	*Versa Module Eurocard*

TABLE OF CONTENTS

1. INTRODUCTION 6
1.1 DOCUMENT SCOPE 6
1.2 THEORY OF OPERATION 6
2. FUNCTIONAL DESCRIPTION 8
2.1 DATA ACQUISITION PROCESS 9
3. DETAILED DESCRIPTION 10
3.1 DATA ACQUISITION INTERFACE - LOW SPEED BUS 10
3.2 DATA ACQUISITION INTERFACE - HIGH SPEED BUS 11
3.2.1 Acquisition of the IF Data 12
3.2.2 Data Transfers 12
3.3 DFB - DISK ARRAY INTERFACE 14
3.4 DSP INTERFACE 14
3.5 PRF DATA BLOCK FORMATTING 14
3.6 DIAGNOSTICS 16
3.7 MTU CONTROL SIGNALS 16
4. TRANSFER PROCESS 17
4.1 INITIALIZATION 17
4.1.1 Power Up Initialization 17
4.1.2 Buffer Initialization 17
4.1.3 Board Initialization 17
4.2 TRANSFER OPERATIONS 18
4.2.1 Transfers to DFB 18
4.2.2 Transfers to DSP 21
4.2.3 Transfers to Both DFB and DSP 23
5. PROGRAMMING MODEL 24
5.1 REGISTER ACCESS 24
5.1.1 DSP Mode Select Register ($0500) 24
5.1.2 Channel Mode Select Register ($0501) 25
5.1.3 DFB Control Register ($0502) 26
5.1.4 DSP Control Register ($0503) 27
5.1.5 Header Words ($0504 to $050B) 28
5.1.6 Spare Register ($050C) 29
5.1.7 Diagnostics ($050D to $051F) 29
6. REFERENCES 32
APPENDIX A - CONNECTOR PIN-OUTS 33
APPENDIX B - TIMING DIAGRAMS 39

LIST OF FIGURES

Figure 1 - EARS Data Acquisition and Control System 7
Figure 2 - DCIB Operating Modes 8
Figure 3 - DCIB Block Diagram 10
Figure 4 - Data Transfers to DFB Flowchart 18
Figure 5 - Multi-Channel Data Transfers to DFB Flowchart 21
Figure 6 - Single Channel Data Transfers to DSP Flowchart 22
Figure 7 - Data Transfers to DFB and DSP Flowchart 23

LIST OF TABLES

Table 1 - DCIB Register Map 24

1. INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes the design of the Data Conversion Interface Board (DCIB) to be used in the Data Conversion System (DCS) of the Experimental Array Radar System (EARS) project. The document includes a high-level description of the system operation and the hardware components. The Data Conversion Interface Board has been developed for the EARS project, as required in Task 11 of contract W7714-4-9858. It has been designed according to MultiDev's proposal and the technical documentation for the disk array, the DSP Board and the DCS Controller Card. See references [1], [2], [3] and [4].

1.2 THEORY OF OPERATION

The present configuration of the EARS data acquisition and control system is shown in Figure 1.

The EARS architecture allows the transfer of massive amount of information between the data sources (IF outputs of the radar vertical and horizontal arrays) and the storage subsystems (hard disk array, Metrum tape unit and Exabyte tape unit). It is also capable of monitoring the transfer activity, set up the radar system for operation and control, and perform some data processing on the radar data.

During a data acquisition session, the Data conversion System receives RF signals from the two antennas at the radar front-end. 16 analog channels are received and down-converted to a centre frequency of 3.5 MHz . Each channel is sampled at 20 MHz with a 12-bit accuracy. Those digitized signals are grouped to increase the data rate and transferred to a disk array via the Differential Fast Bus (DFB). Once the information is stored on disk at full speed (20 MB/sec), the acquired information is backed-up on tape to free the disk array for another session.

The proposed Data Conversion Interface Board will be able to collect data from groups of four channels and transfer 4, 8 or 16 channels to the disk array. The group(s) will be user selectable. In addition, the DCIB will be able to send data to DSP cards. Any single channel, or groups of 4, 8 or 16 channels (the same data being sent over the DFB) will be sent to the DSP card.

The data transfer mechanism is executed in two phases. During the first phase, the system acquires the data from all 16 channels and temporarily stores the data inside the AtoD Board memory buffers. When the memory buffers are full, the DCIB stops the data acquisition process.

The second phase reads the digitized data from the AtoD Boards and transfers the data (in groups of 4, 8 or 16 channels) to the disk array and/or to the DSP Board. The information is transferred until the memory buffers are empty. A new cycle can then begin.

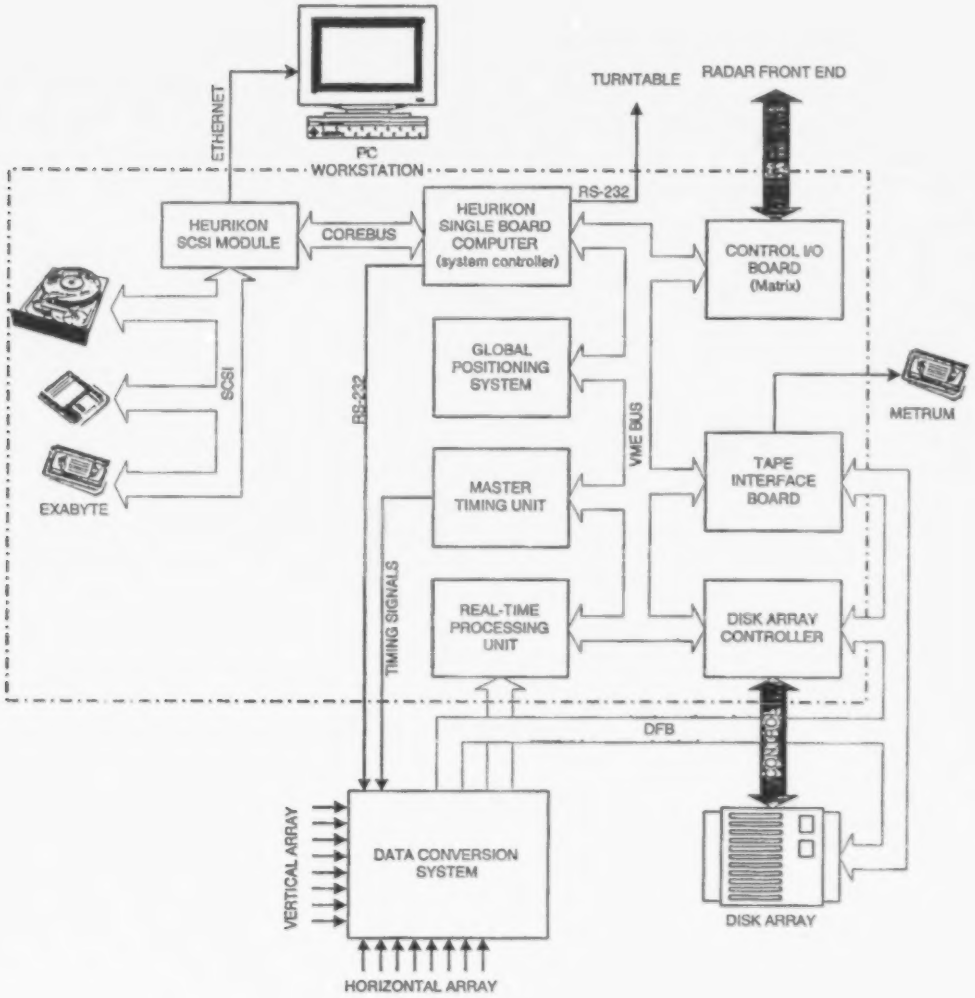


Figure 1 - EARS Data Acquisition and Control System

2. FUNCTIONAL DESCRIPTION

The DCIB is designed to allow transfers between the 16 AtoD Boards (12-bit data streams) and the disk array and/or the Real-Time DSP Card. Three modes of operations are supported (see Figure 2). In the first mode, the interface card reads data from 4, 8 or 16 AtoD Boards and transfers the data to the disk array via the DFB at a maximum sustained rate of 10 MHz (20 MB/sec, 16-bit words). In the second mode of operation, the interface card reads data from 2, 4, 8 or 16 channels and transfers the data to the DSP card at a maximum sustained rate of 6.67 MHz (26.7 MB/sec for 32-bit words containing 24 data bits). The third mode is the combination of modes 1 and 2: data is sent to both the DSP card and the disk array. The data sent to the DSP is either the same as that sent to the disk array, or two channels selected from the data sent to the disk array.

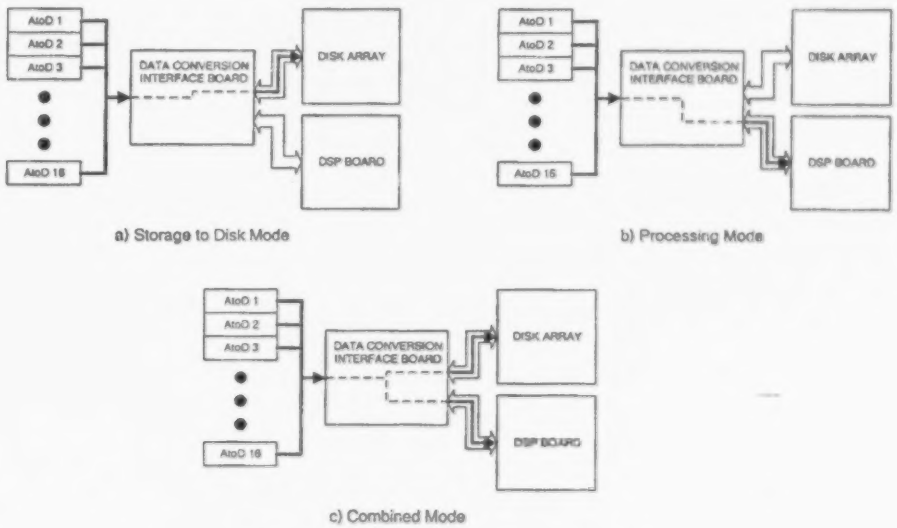


Figure 2 - DCIB Operating Modes

The board is designed to conform to the High Speed and Low Speed Buses [4] using a VME type of backplane, the DFB standard as defined by Storage Concept (for the disk array) [2], and the data interface protocol of the IXI32D mezzanine card residing on the Ixthos DSP card [3]. The High Speed and Low Speed Buses are proprietary buses defined for the EARS DCS. The High Speed Bus propagates radar data while the Low Speed Bus handles the control and status registers.

2.1 DATA ACQUISITION PROCESS

The data acquisition procedure is done in two phases, the acquisition phase and the data transfer phase, both managed by the Data Conversion Interface Board. When the radar is active, the AtoD Boards convert the analog IF signals coming from the 16 channels. The 16 IF input channels are sampled when the MTU sends sampling timing signals directly to the AtoD Boards (these signals are a combination of a sampling clock and an "acquisition window" signal which enables data sampling).

During the acquisition phase, the DCIB sends addresses over the backplane to indicate where the samples will be stored on the AtoD board memory buffers. The DCIB is responsible for providing the addresses, although the memory is located on the AtoD Boards. The Master Timing Unit provides the sampling clock to the AtoD Boards. At the maximum 20 MHz clock rate, a write cycle is performed every 50 nsec for each of the 16 AtoD Boards.

When the acquisition phase is complete, the memory buffers are full and become available for transfers. The DCS controller Card disables the data sampling on the AtoD Cards. The DCIB starts issuing addresses to extract the data from the AtoD memory buffers and transfer the information to the disk array and/or the DSP Card until the memory buffers become empty. A new acquisition cycle can begin.

3. DETAILED DESCRIPTION

The following section describes in details the operation of the different sections of the Data Conversion Interface Board:

- the data acquisition interface, comprised of the Low Speed Bus and the High Speed Bus,
- the disk array interface, via the DFB (Differential Fast Bus),
- the DSP interface (IXI32D mezzanine card),
- the data block formatting,
- the diagnostics, and
- the other I/O signals.

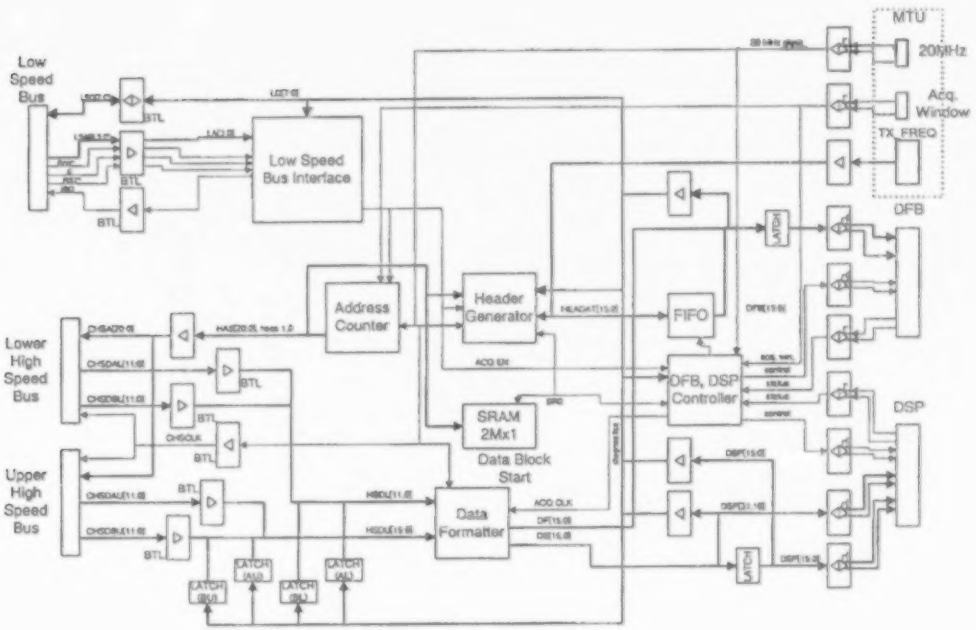


Figure 3 - DCIB Block Diagram

3.1 DATA ACQUISITION INTERFACE - LOW SPEED BUS

The Low Speed Bus connects the DCS Controller Card to the DCIB. It is used by the Controller Card to address the DCIB control and status registers. Four control registers are provided for the DFB and DSP control logic (see sections 5.1.1 to 5.1.4). The first register is responsible for selecting the AtoD channels to be transferred to the DSP and the second register is responsible for selecting the AtoD channels to be transferred to the DFB.

The third register is dedicated to the DFB and controls the following:

- start and stop acquisition
- acquire data or transfer data to DFB
- enable interrupts: AtoD memory buffer full and AtoD memory buffer empty

The fourth register controls the DSP interface and other functions:

- DSP slave address select
- Transfer to DSP error
- DSP reset
- Header FIFO reset
- DCIB reset
- Header (PRF Data Block Start) bit

The Low Speed Bus is an extension of the 68HC11 microcontroller bus on the DCS Controller Card. The read and write cycles are executed directly from the 68HC11 memory map (addresses $0500 to $051F). Please refer to section 5 for details on the register bit assignments.

3.2 DATA ACQUISITION INTERFACE - HIGH SPEED BUS

The High Speed Bus connects the 16 AtoD cards to the DCIB. Two buses are provided: the Lower High Speed Bus (located on the lower connector on the backplane) and the Upper High Speed Bus (upper connector). Each bus has 21 address bits, 2 group select bits, 24 data bits, one sampling clock signal. The data bus is divided into two 12-bit data paths (paths A and B).

The DCIB is responsible for generating addresses during both the data acquisition phase (the 16 IF channels are sampled by the AtoD Boards) and the data transfer phase (the digitized samples are read by the DCIB and sent to the disk array and/or the DSP board). During the acquisition phase, a counter provides 21-bit addresses to all 16 channels to store the samples in sequence into the AtoD buffer memory. No memory reads and no data transfer activity are allowed while the samples are being written to memory.

At the end of the data acquisition period, when the buffer memory is full, the counter is reset and starts generating 21-bit addresses to extract samples that were previously stored into the memory buffers. The samples are then transferred to the disk array and/or to the DSP board. When all data has been transferred, a new acquisition phase starts and the counter is reset.

During each read cycle, 48-bit wide data words are read from the AtoD Boards. Four 12-bit channel data words are simultaneously received by the DCIB, two channels on the upper bus and two on the lower bus. The data is then formatted and sent to the DFB or the DSP.

3.2.1 Acquisition of the IF Data

A data acquisition cycle is enabled each time the MTU activates the Acquisition Window signal. When this signal is activated, the DCIB starts sending the counter address over the high-speed bus. The counter always writes to the next available address and increments by one after each write cycle. At the beginning of the acquisition phase, this counter is reset.

The counter clock comes from the MTU which is either synchronized with an external clock (usually a reference signal coming from the radar front-end), or its own programmable internal clock. If the maximum 20 MHz frequency is programmed, one write cycle is performed every 50 nsec. This signal is sent to the 16 AtoD cards and all 16 channels are sampled at the same time.

3.2.2 Data Transfers

The DCIB manages the data transfers between the AtoD boards and the DCIB bus interfaces. The 16 AtoD Boards are available to the DCIB in groups of four channels (channels 1 to 4, 5 to 8, 9 to 12 and 13 to 16). One group of four channels is transferred to the DCIB over the backplane as one 48-bit word. The DCIB can send only one group, two groups or all four groups to the disk array or to the DSP card.

The data received from the AtoD Boards is encoded by the backplane as one 48-bit word composed of the Upper A and Upper B data paths (each path is 12 bits wide and located on the upper connector), and the Lower A and Lower B data paths (each path is 12 bits wide and located on the lower connector). The channel distribution is shown below:

Bits	Data	Group 1	Group 2	Group 3	Group 4
Upper A (0 to 11)	first channel	ch. 1	ch. 5	ch. 9	ch. 13
Lower A (0 to 11)	second channel	ch. 2	ch. 6	ch. 10	ch. 14
Upper B (0 to 11)	third channel	ch. 3	ch. 7	ch. 11	ch. 15
Lower B (0 to 11)	fourth channel	ch. 4	ch. 8	ch. 12	ch. 16

3.2.2.1 Transfers to the Disk Array

When one 48-bit word is read, the channel data is packed into three words of 16 bits each for their transfer to the disk array over the DFB (16-bit wide bus). The data packing of each 48-bit word is as follows:

Word	Data
1	D15-D4 = first channel (bits 11 to 0) D3-D0= second channel (bits 11 to 8)
2	D15-D8 = second channel (bits 7 to 0) D7-D0 = third channel (bits 11 to 4)
3	D15-D12 = third channel (bits 3 to 0) D11-D0 = fourth channel (bits 11 to 0)

When four channels are selected, the same group is always read from the AtoD Boards. When eight channels are selected, two read cycles are necessary to read two groups of four channels. When all 16 channels are selected, four consecutive read cycles are necessary.

The maximum transfer rate of the DFB is 20 MB/sec (one 16-bit word every 100 nsec). Therefore, one 48-bit word is read from the High Speed Bus every 300 nsec (20 MB/sec).

3.2.2.2 Transfers to the DSP Board

The transfers to the DSP Board are very similar to those to the DFB, with the exception of the data packing that uses a different scheme. When groups of channels are sent to the DSP board (if the disk array interface is enabled, the groups must be the same), each channel is coded as shown in the next table and combined two-by-two to form a 32-bit word.

Word	Bits	Data	Group 1	Group 2	Group 3	Group 4
N	0 to 11	sample one	ch. 1	ch. 5	ch. 9	ch. 13
	12 to 15	group number				
	16 to 27	sample two	ch. 2	ch. 6	ch. 10	ch. 14
	30	0 (multi-channel)				
	31	1 = new PRF				
N+1	0 to 11	sample three	ch. 3	ch. 7	ch. 11	ch. 15
	12 to 15	group number				
	16 to 27	sample four	ch. 4	ch. 8	ch. 12	ch. 16
	30	0 (multi-channel)				
	31	0 = same PRF				

Transfers to the DSP Board can be done with 2, 4, 8 or 16 channels. For 4, 8 or 16 channels, the selected channels must be the same as those sent to the disk array, if the DFB transfer mode is enabled. Since one 48-bit word is acquired every 300 nsec, two 32-bit words containing two channels each must be sent to the DSP every 300 nsec (one 32-bit word every 150 nsec).

For the dual channel transfer mode, bit 30 has a different assignment.

Word	Bits	Data	Group 1	Group 2	Group 3	Group 4
N	0 to 11	sample one	ch. 1 or 3	ch. 5 or 7	ch. 9 or 11	ch. 13 or 15
	12 to 15	channel number				
	16 to 27	sample two	ch. 2 or 4	ch. 6 or 8	ch. 10 or 12	ch. 14 or 16
	30	1 (dual channel)				
	31	1 = new PRF				

3.3 DFB - DISK ARRAY INTERFACE

The disk array interface implements the DFB standard as defined by Storage Concept in reference [2]. The interface recognizes and generates signals from/to the Differential Fast Bus control lines and informs the main control logic of the state of the Differential Fast Bus.

The DFB control logic provides all the signaling required to perform the following operations:

- manage the control signals on the DFB for master mode operation.
- manage the write cycles from the buffer memory on the Data Conversion Interface Board to the destination device on the DFB. The destination device is the disk array.

After setting the direction (or operation mode), the disk array frame size (288 KB) and enabling the Differential Fast Bus mastership bit in the control register (section 5.1.3), the disk array transfer can be initiated via the Disk Array Controller. From that point on, the process is automatic (see reference [2]).

3.4 DSP INTERFACE

The DSP interface implements the protocol as defined by Ixthos for the IXI32D Mezzanine Board in reference [3]. The interface recognizes and generates signals from/to the DSP bus control lines and informs the main control logic of the state of the DSP subsystem.

The DSP control logic provides all the signaling required to perform the following operations:

- manage the control signals on the DSP bus for master mode operation.
- manage the write cycles from the Data Acquisition Interface Board output latch to the DSP Mezzanine Board IXI32D.

After setting the operation mode and enabling the DSP interface bit in the control register (section 5.1.1), the DSP transfer can be initiated by the DCIB. From that point on, the process is controlled by the DCIB, as per reference [3]. If the DSP Card does not empty the DSP Mezzanine Board buffer fast enough, a DSP error interrupt will eventually be generated. This bit is available in the DSP Control Register (section 5.1.4).

3.5 PRF DATA BLOCK FORMATTING

A PRF Data Block is defined as a group of samples acquired during the same PRF. The acquisition of data within the same PRF is enabled by the Acquisition Window signal coming from the MTU.

The formatting of the data blocks transferred to the DFB and DSP interfaces is done during both the acquisition and data transfer phases. During the acquisition phase, the

header information to be included with each PRF data block is prepared and temporarily stored in FIFO's. When the acquisition phase is complete and the data transfers start, the data to be transferred is packed and grouped into PRF data blocks. The header information prepared during the acquisition phase is then added at the beginning of each PRF data block.

The PRF data blocks are composed of a header and the PRF samples. The header contains the necessary information to extract the radar data (see section 5.1.5). The header includes the following information:

Word	Data
1	Header Reference Word
2	Sample Count Word
3	Data Block Status Register
4	Event Word
5+	radar data (see section 3.2.2.2)

The header is followed by the radar data. The size of the buffer can be determined by multiplying the sample count by the number of channels contained in the data block.

$$size = channel\,mode * sample\,count * \frac{3\ packed\ words}{4\ samples} + 4\ header\ words$$

For example, if the sample count is 133 and the channel mode specifies 8 channels (see section 5.1.2 for more details), the buffer size is 802 words of 16 bits. The data packing scheme is explained in section 3.2.2.1.

In order to include the information in the header at the right time, the header must be prepared during the acquisition phase and stored in a FIFO. Since there can be multiple PRF's during the acquisition phase (if 133 samples are acquired per PRF, approximately 2000 PRFs are required to fill the 256K AtoD board memory), a large FIFO (32KB) is required and a synchronization mechanism must be developed to insert the header at the beginning of each new PRF data block when the data is transferred to the DFB.

The header tracking mechanism is done with a 1-bit SRAM chip that uses the same address counter than the high speed bus for the data acquisition. When a new PRF starts, the control logic writes a one to the address, meaning that a new PRF starts here. At the same time a new header is prepared. When the acquisition is complete, the counter is reset and the data transfers start (see appendix B for the Timing Diagrams).

During the data transfer phase, the DCIB reads 48-bit words from the high speed bus using the address counter. At the same time the address counter also provides the address of the SRAM chip. When a one is issued by the SRAM, a new PRF occurred at this address and the DCIB inserts the header words before it can continue to read the new PRF data. The number of headers stored in the FIFO's during the acquisition phase shall correspond to the number of set bits in the SRAM chip.

3.6 DIAGNOSTICS

The verification of the board functionality is done via a number of latches and buffers that read and store the data information on the buses and interfaces. The diagnostics information can be obtained from the DCS Controller Card via the Low Speed Bus. Four groups of diagnostics registers can be accessed:

- The *data counter*, which is usually monitored to detect if the counter is incrementing during the acquisition and data transfer phases. Four read-only bytes are allocated to the 21-bit counter.
- The 32-bit *DSP data word*, which corresponds to the data being sent to the DSP Mezzanine Card. Four read-only bytes are allocated to this word.
- The 16-bit *DFB data word*, which corresponds to the data being sent to the DFB by the DFB interface. Two read-only bytes are allocated to this word.
- The 48-bit *sample word*. This register is used to latch simulated data into the data formatter input to verify the proper functionality of the board. Eight write-only bytes are allocated to this word.
- In addition to these diagnostic registers, the DSP Control Register contains the SRAM data bit which allows the detection of a new PRF.

The Diagnostics Status Register is used to enable the diagnostics mode. A more detailed description of the diagnostic registers is provided in section 5.1.7.

3.7 MTU CONTROL SIGNALS

Aside from the buses specified above, three control signals are provided by the Master Timing Unit: the 20 MHz clock, the Acquisition Window signal and the Event bits.

The 20 MHz reference clock is used by the DCIB for many purposes. It is sent to all 16 AtoD boards to synchronize the sampling cycles. It is also used to increment the address counter which supplies the addresses to the AtoD buffer memory. The addresses are synchronized to the sampling clock. Finally it synchronizes the data formatting function during the date transfer cycles.

The Acquisition Window signal is used by the DCIB to enable the address generation during the acquisition phase. When this signal is raised, a new PRF starts, a header is generated, the address counter is enabled and samples are stored into the AtoD buffer memory. When it is cleared, the acquisition is suspended. The rising edge of this signal indicates a new PRF.

The Event bits are available to the DCIB on a special 16-bit input bus. Each time a new header is generated, these bits are read and included in the header. Since these bits could be updated every PRF, a high speed parallel port on the MTU will be dedicated to this task.

4. TRANSFER PROCESS

The following section describes the proper sequence to follow when transferring data. The process is divided in two sections: Initialization and transfer operations.

4.1 INITIALIZATION

The initialization of the Data Conversion Interface Board should be performed before beginning any transfers. The DCIB initialization can be divided into three sections: Power up initialization, FIFO buffer initialization and board initialization.

4.1.1 Power Up Initialization

When the system is powered up, the DCIB is automatically reset to a known, idle state. The Differential Fast Bus interface signals are placed in high impedance (DFB MSTR is cleared, section 5.1.3). The DSP interface is in idle mode. The header FIFO is reset (FIFO Empty Flag asserted, FIFO Full Flag is reset). The AtoD buffer full and empty interrupts are disabled (section 5.1.7.1). The acquisition is disabled and DFB transfers are disabled (section 5.1.3). The diagnostics are also disabled (section 5.1.7.1).

A board reset can be executed at any time by setting the DCIB reset bit in the DSP control register (section 5.1.4).

4.1.2 Buffer Initialization

The header and DSP FIFO buffers can be initialized via software at any time. It is recommended that, anytime a data acquisition session is to occur, the buffers be initialized. During transfers, if the buffer sequencing gets corrupted, the FIFO might need to be placed in a known state. Resetting the FIFO ensures proper operation for the transfer to come.

Header and DFB buffer initialization is performed when setting D5 of the DSP control Register (see section 5.1.4). DSP buffer initialization (the FIFO's are on the Mezzanine card) is done when setting D3 of the DSP Control Register. This raises the ATTN signal on the DSP interface which will reset the DSP Mezzanine Card and the DSP Card (section 5.1.4).

4.1.3 Board Initialization

Board initialization is required to ensure correct transfer procedures. A complete board initialization is accomplished by setting D6 of the DSP Control Register (see section 5.1.4). Following this action, the card and its associated interfaces are placed in an idle state. To accomplish data transfers, the board must have all the appropriate bits set following this reset.

Individual interfaces can be reset separately if this is required. Setting the appropriate bit will reset the individual interface. Refer to section 5.1.4 for more details on resetting individual interfaces.

4.2 TRANSFER OPERATIONS

The following section describes what processes are required in order to accomplish successful transfers. A complete data storage cycle is accomplished in two phases: an acquisition phase, which temporarily stores the digitized samples into the AtoD buffer memory, and the data transfer phase, which transfers the data from the AtoD memory to the disk array via the DFB and/or to the DSP card via the DSP Mezzanine Board.

As described in section 2, three modes are possible: transfers to the DFB, transfers to the DSP and transfers to both.

4.2.1 Transfers to DFB

The transfers to the disk array are managed by the control registers and by the MTU timing signals. Before the data transfers to DFB are enabled, it is recommended to reset the DCIB by setting and resetting the DCIB RESET bit in the DSP Control Register (location $0503).

The Data Transfers to DFB flowchart is shown below.

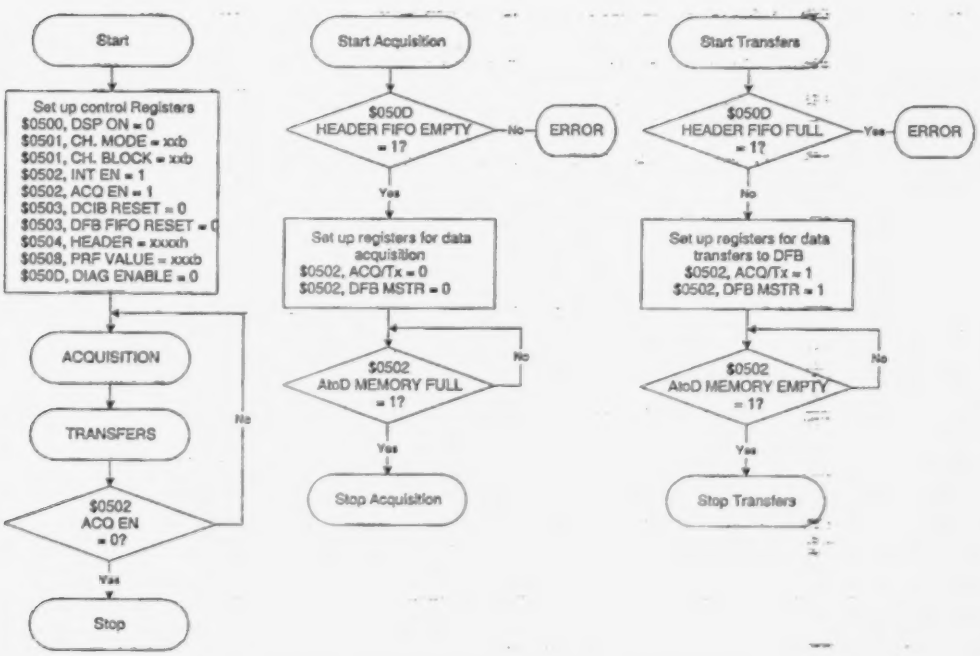


Figure 4 - Data Transfers to DFB Flowchart

Transfers to DFB are initiated by the DCS Controller Card which sets up the control registers and enables the data transfers. Once the control registers are set up, the MTU timing signals automatically clock the address counter which will fill up and empty the AtoD buffer memory during the acquisition and data transfer phases respectively.

The transfers to DFB are stopped when the DCS Controller Board clears the acquisition enable bit (ACQ EN = 0 in the DFB Control Register, location $0502). The DCIB completes the transfer cycle and then stops its activities. The data transfers to DFB can also stop if the DCIB detects an error during the transfers. Errors can be of two types:

- The header FIFO is not empty at the beginning of a cycle. There is a mismatch in the number of headers and the number of PRF data blocks.
- The header FIFO is full. The number of PRF data blocks exceeded the capacity of the header FIFO.

When an error occurs, an interrupt is sent to the DCS Controller Card.

4.2.1.1 Transfer Initialization

Before the data transfers to DFB can occur, the DCIB control registers must be initialized as shown in Figure 4.

- The DSP interface is disabled.
- The channel mode and channel blocks are selected. Refer to section 5.1.2 for details.
- The AtoD buffer memory full and empty interrupts are enabled.
- The Header Reference word is written, if required. This word will become the reference each time a new PRF data block is stored to disk.
- The PRF value is written. The system operator enters the PRF value into the console which transfers it to the DCIB via the system controller and the DCS Controller Card.
- Finally, the Acquisition Enable bit is set.

4.2.1.2 Acquisition

When the Acquisition Enable bit is set, the DCIB starts the acquisition phase by resetting the address counter. The header FIFO must be empty. If the FIFO is not empty, there has been a mismatch in the number of PRF data blocks and the number of headers and an error is generated.

The DCIB provides the sampling clock to the AtoD converters. See Appendix B for the Acquisition Phase Timing Diagram. The sampling clock is the 20 MHz clock signal coming from the MTU. This sampling clock triggers the AtoD converters, the DCIB address counter providing the address to the AtoD memory buffers as well as the address to the SRAM indicating the presence of a new PRF.

The acquisition phase starts filling the AtoD memory buffers by sending the address over the high speed bus. The acquisition always starts on the rising edge of the Acquisition Window signal in order to collect complete PRF data blocks.

Each time the Acquisition Window signal rises, a new PRF starts and a "one" is written into the SRAM at this address. Since the acquisition phase always starts with a new PRF data block, the SRAM bit is always a "one" at address zero.

The header block is written to the header FIFO at the end of a PRF data block. On the rising edge of the next acquisition window, the header words from the previous data block, available at locations $0504 to $050B (see section 5.1.5), are copied into the FIFO. At the same time, the Sample Count Register is calculated by the DCIB (address counter at the end of the PRF minus the address counter at the beginning of the PRF) and stored at location $0506.

When the AtoD buffer memory is full, i.e. the address counter has reached the last address of the AtoD memory, the DCIB stops generating addresses and the sampling clock. The last header block is written into the header FIFO. The last PRF data block is usually incomplete and the Non Valid PRF bit is set in the Data block status register ($0508) to indicate this state.

The acquisition phase is complete and the data transfers phase can start.

4.2.1.3 Data Transfers to DFB

When the AtoD memory is full, the DCIB disables the sample clock going to the AtoD cards and resets the address counter. As shown in Figure 4, the Acquisition or Transmit bit is set to indicate data transfers mode and the DFB Master bit is set to initiate data transfers to the disk array. See Appendix B for the Data Transfer Phase Timing Diagram.

The first four 16-bit words to be sent to the DFB are normally the first header block stored in the header FIFO. The SRAM's bit at address zero should be a "one", indicating the start of a new PRF data block. Following the header block, the DCIB starts sending the samples in sequence.

Depending on the channel mode and block settings (register $0501), one, two or four channel group read cycles might be required. If four channels are read, only one high speed bus read cycle is required. Every read cycle brings 48-bit (4 channels) of data on the Upper and Lower Data buses. Two high speed bus channel select (HSCS) bits generated by the address counter will select one of four channel groups: channels 1 to 4, 5 to 8, 9 to 12 or 13 to 16. The address counter increments after each read cycle and the HSCS bits do not change state during the data transfers phase.

If two groups are selected, two high speed bus read cycles are required. Channels 1 to 8 or 9 to 16 are read. The address counter increments every second read cycle and the HSCS bits alternate between group 1 and 2, or between 3 and 4, after each read cycle.

If all four groups are selected, four high speed bus read cycles are required. Channels 1 to 16 are read. The address counter increments every fourth read cycle and the HSCS bits select each group in sequence after each read cycle.

Each time the address counter increments the address by one, the SRAM bit is verified to detect the presence of a new PRF data block. If this bit is set, the sample data transfers are suspended and a new header block from the header FIFO is inserted in the data transfers. After the four header words are sent, the sample data transfers can resume.

The four 12-bit sample data are formatted before they are sent over the DFB to the disk array. The packing format is shown in section 3.2.2.1.

When the address counter reaches the last address of the AtoD buffer memory, the data transfers stop and the DCIB is ready for a new acquisition phase.

4.2.1.4 End of Transfers

The data transfer process is stopped when the DCS Controller Card clears the Acquisition Enable bit (location $0502). This bit is read to detect the end of data transfers after each data transfers phase.

4.2.2 Transfers to DSP

The transfers to the DSP Mezzanine Card are very similar in many aspects to the transfers to DFB. They are also managed by the control registers and by the MTU timing signals. Before the data transfers to DSP are enabled, it is recommended to reset the DCIB by setting and resetting the DCIB RESET bit in the DSP Control Register (location $0503).

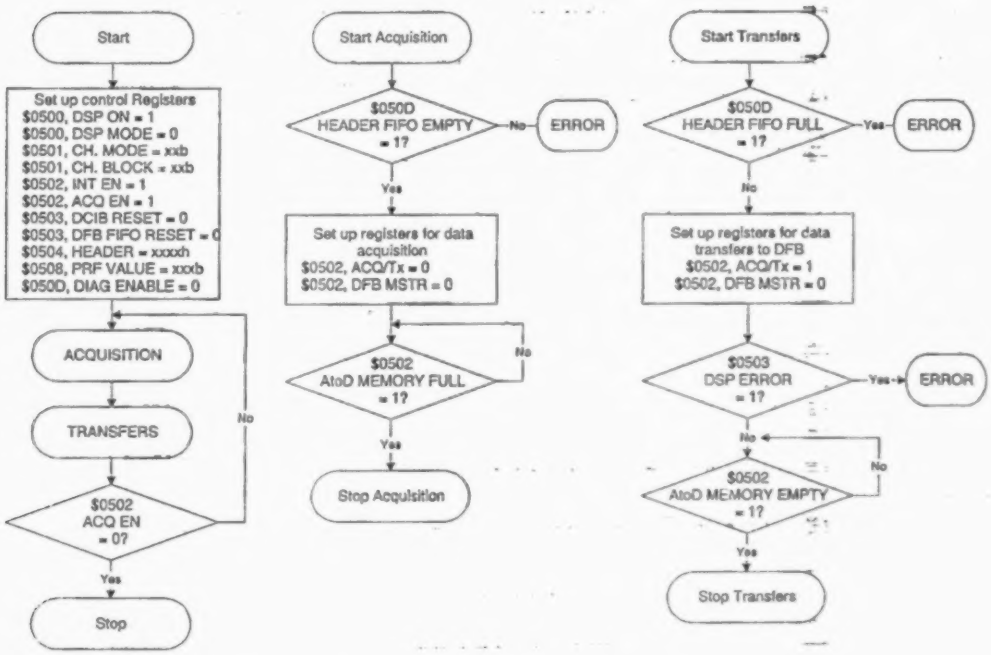


Figure 5 - Multi-Channel Data Transfers to DFB Flowchart

4.2.2.1 Multi-Channel Data Transfers

The Data Transfers to DSP flowchart is shown in Figure 5. The only difference between the transfers to DSP and transfers to DFB are the DSP ON bit which is set and the DFB Master bit which is cleared. Aside from the change in those two bits, all operations are the same. At the beginning of a new PRF Data Block (when the SRAM bit is set), D31 of the DSP Data Word is set (see section 3.2.2.2).

Please note that there is no DSP FIFO's. They are instead located inside the DSP Mezzanine Card. If the FIFO's fill up, a DSP error (section 5.1.4) is generated and the DCIB suspends the data transfers.

4.2.2.2 Dual Channel Data Transfers

If only two channels are transferred to the DSP, the DSP Mode Select Register must be updated to select the Dual Channel Mode and the channel number. At the beginning of a new PRF Data Block (when the SRAM bit is set), D31 of the DSP Data Word is set (see section 3.2.2.2).

Please note that the channel number must be part of the group(s) selected in the Channel Mode Select Register ($0501). Otherwise, the channel number will be modified by the DCIB to be included in the selected group(s).

In the case of single channel data transfers, the data format differs from the multi-channel data transfers. Refer to section 3.2.2.2.

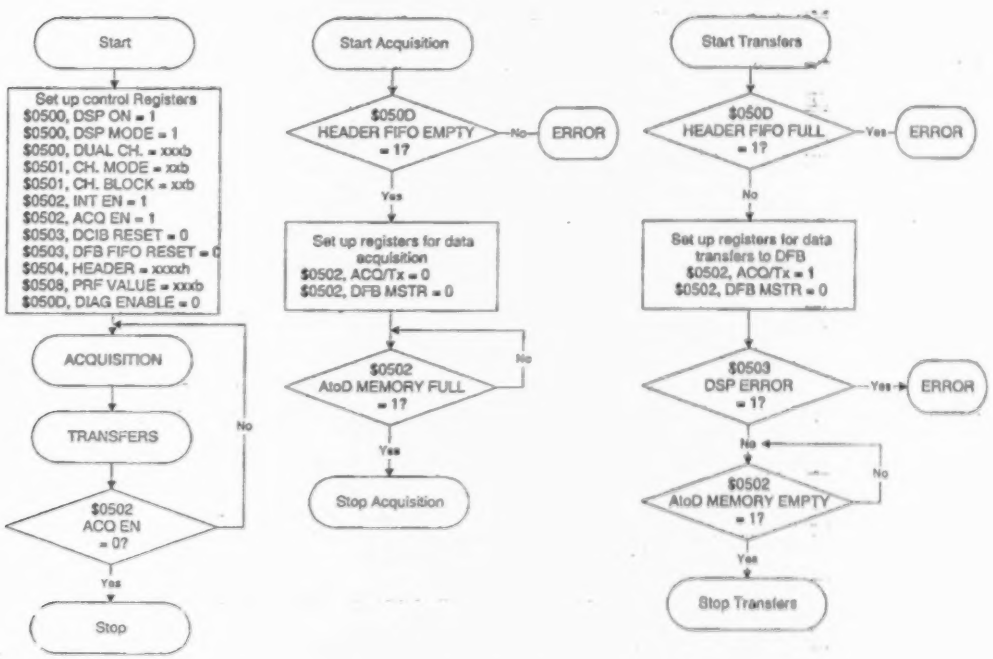


Figure 6 - Single Channel Data Transfers to DSP Flowchart

4.2.3 Transfers to Both DFB and DSP

The transfers to both interfaces is done in parallel and therefore do not influence each other's protocol. The only limitation to the data transfers is the selection of the channel groups which shall be the same for the DFB and the DSP (location $0501).

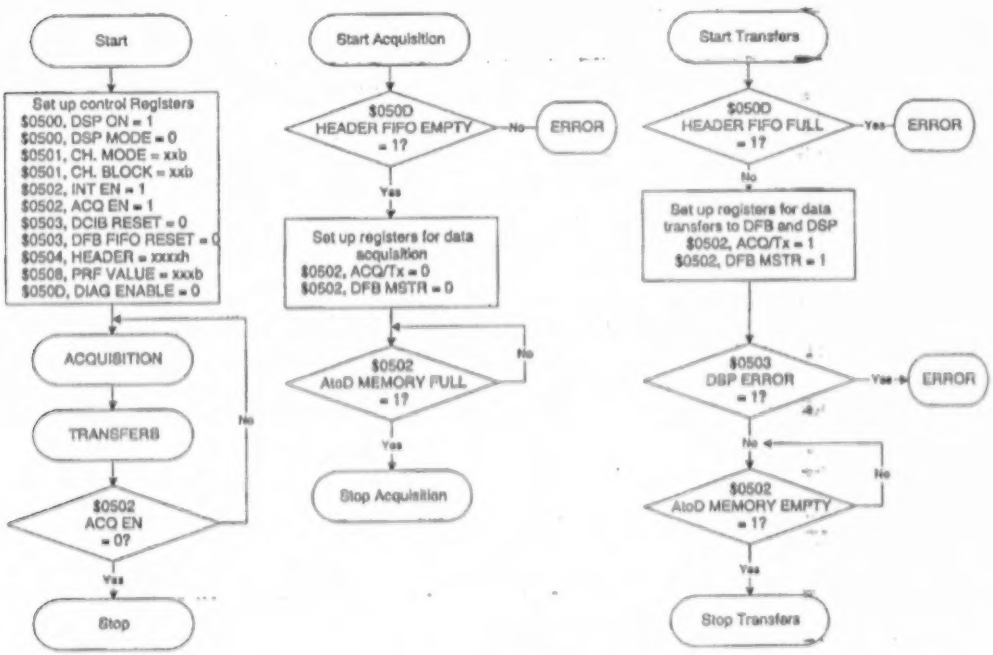


Figure 7 - Data Transfers to DFB and DSP Flowchart

5. PROGRAMMING MODEL

The following section describes in details the ports and registers available under program control.

5.1 REGISTER ACCESS

All registers are accessed via the Low Speed Bus from the DCS Controller Card. The registers are memory mapped to the 68HC11 address space between $0500 and $051F. The list of registers is shown below.

Address	Description	Width (Bits)
$0500	DSP Mode Select Register	8
$0501	Channel Mode Select Register	8
$0502	DFB Control Register	8
$0503	DSP Control Register	8
$0504	Header Reference Word	16
$0506	Sample Count Word	16
$0508	Data Block Status Register	8
$0509	Spare Register	8
$050A	Event Word	16
$050C	Spare Register	8
$050D	Diagnostics Status Register	8
$050E	DFB Data word	16
$0510	DSP Data Word	32
$0514	Data Block Address Counter	32
$0518	Upper A Sample (first channel sample)	16
$051A	Lower A Sample (second channel sample)	16
$051C	Upper B Sample (third channel sample)	16
$051E	Lower B Sample (fourth channel sample)	16

Table 1 - DCIB Register Map

5.1.1 DSP Mode Select Register ($0500)

The DSP Mode Select Register selects the data channel or channels to be sent to the DSP interface. If the dual channel mode is chosen, only two channels from the data channels selected in the Channel Mode Select Register are transferred. If the multiple channel mode is chosen, all data channel selected in the Channel Mode Select Register are transferred.

	D7	D6	D5	D4	D3	D2	D1	D0
$0500	X	X	DSP ON	DSP MODE	DUAL CHANNEL			

5.1.1.1 DSP On (D5)

The DSP ON bit enables or disables the data transfers to the DSP Mezzanine Card.

Bit	Function
5	DSP Interface Enable 0 - disabled 1 - enabled

5.1.1.2 DSP Mode (D4 to D0)

The DSP Mode bit selects the transfer of two or multiple channels. If two channels are selected D0 to D3 provide the channel numbers.

Bit	Function
4	DSP Mode 0 - all channels (see $0501) 1 - dual channel
0 to 3	Channel number*

* if the Channel Mode bits in the Channel Mode Select Register select one group (4 channels), the Channel Mode bits will be forced into D2 and D3 of the Channel Number bits (to select a valid channel number from the data being read). If the Channel Mode bits in the Channel Mode Select Register select two groups (8 channels), Channel Mode bit D3 will be forced into D3 of the Channel Number bits. D0 is always set to 0.

5.1.2 Channel Mode Select Register ($0501)

The Channel Mode Select Register selects the data channels to be sent to both DFB and DSP interfaces (if the DSP is active and the multiple channel mode is selected in the DSP Mode Select Register).

	D7	D6	D5	D4	D3	D2	D1	D0
$0501	X	X	X	X	CHANNEL MODE		CHANNEL BLOCK	

5.1.2.1 Channel select (D3 to D0)

The channel selection is done by the Channel Mode bits and the Channel Block bits. The Channel Mode bits select the data transfer of one, two or four channel groups. The Channel Block bits select the channel group(s) to be transferred.

Bit	Function
3 and 2	Channel Mode 00 - invalid selection 01 - one group, 4 channels 10 - two groups, 8 channels 11 - all 16 channels
1 and 0	Channel Blocks (if channel mode = 01) 00 - channels 1 to 4 01 - channels 5 to 8 10 - channels 9 to 12 11 - channels 13 to 16 Channels Blocks (if channel mode = 10) 0X - channels 1 to 8 1X - channels 9 to 16

5.1.3 DFB Control Register ($0502)

The DFB Control Register provides all the control bits to set-up the data transfers to the DFB interface.

	D7	D6	D5	D4	D3	D2	D1	D0
$0502	INT EN	AtoD FULL	AtoD EMPTY	X	X	ACQ/Tx	ACQ EN	DFB MSTR

5.1.3.1 Interrupts (D7, D6 and D5)

Five interrupts are generated by the DCIB: the AtoD memory buffer full and AtoD memory buffer empty, available on this register, the header FIFO full and header FIFO empty, available at location $050D (section 5.1.7.1), and DSP error, available at location $0503 (section 5.1.4).

When the AtoD memory buffer is full, the memory is ready for data transfers; when empty, the memory is ready for another acquisition phase.

Bit	Function
7	Interrupts 0 - disabled 1 - enabled
6	AtoD memory full (read only) 0 - not full 1 - full and ready for data transfer
5	AtoD memory empty (read only) 0 - not empty 1 - empty and ready for acquisition

5.1.3.2 Data Transfers (D2, D1 and D0)

The Data Transfer Control bits enable the acquisition, indicate the status of the DCIB activity (acquisition or data transfers) and enable the DFB for transfers.

Bit	Function
2	Acquisition/data transfers select 0 - acquisition 1 - data transfers
1	Acquisition enable 0 - disabled 1 - enabled
0	DFB Master enable 0 - DFB disabled 1 - DFB mastership enabled for transfers

5.1.4 DSP Control Register ($0503)

The DSP Control Register provides all the control bits to set-up the DSP interface and initialize the DCIB.

	D7	D6	D5	D4	D3	D2	D1	D0
$0503	SRAM DATA	DCIB RESET	HEADER FIFO RESET	X	DSP ATTN CTL	DSP ERROR	DSP SLAVE ADDRESS	

5.1.4.1 SRAM Data (D7)

The SRAM status bit is provided by the SRAM chip and is used to indicate when a new PRF has started. This read only bit is set when a new PRF begins.

Bit	Function
7	SRAM data bit (read only) 0 - same PRF data 1 - new PRF has started at this address

5.1.4.2 Reset Bits (D6, D5 and D3)

Three reset bits are provided to reset the DCIB, the Header FIFO buffer and the DSP Mezzanine Card.

Bit	Function
6	DCIB reset 0 - no reset 1 - reset
5	Header FIFO reset 0 - no reset 1 - reset
3	DSP ATTN control 0 - no reset 1 - ATTN is set, reset the DSP bus

5.1.4.3 DSP Error (D2)

The DSP error bit indicates the status of the Mezzanine Card. When set, the Mezzanine Card does not empty its FIFO and a buffer overflow occurred.

Bit	Function
2	DSP error 0 - no overflow 1 - DSP Mezzanine Card overflow

5.1.4.4 DSP Slave Address (D1 and D0)

These two bits are used to select the DSP Mezzanine Card. The number must be the same than the one allocated to the DSP Mezzanine Card.

Bit	Function
1 and 0	DSP slave address xx - Mezzanine Card slave address

5.1.5 Header Words ($0504 to $050B)

The header included at the beginning of each PRF data block can be read in registers $0504 to $050B. All registers are read only, except the 16-bit header reference word which is selected by the user, and the Data Block Status Byte which can modify the channel mode and the PRF bits.

5.1.5.1 Header Reference Word ($0504 and $050B)

The 16-bit Header Reference Word is used to indicate the beginning of a new PRF data block.

	D7	D6	D5	D4	D3	D2	D1	D0
$0504	D15	D14	D13	D12	D11	D10	D9	D8
$0505	D7	D6	D5	D4	D3	D2	D1	D0

5.1.5.2 Sample Count Word ($0506 and $0507)

The 16-bit Sample Count Word is used to indicate the size of the PRF data block. The size is determined by the equation in section 3.5. This is a read only word

	D7	D6	D5	D4	D3	D2	D1	D0
$0506	D15	D14	D13	D12	D11	D10	D9	D8
$0507	D7	D6	D5	D4	D3	D2	D1	D0

5.1.5.3 Data Block Status Register ($0508)

The Data Block Status Register is used to control the data channels included in the PRF data block and the PRF value. If the PRF data block is incomplete (i.e. it is the last data block stored in the AtoD memory buffer and it is not complete), the Non Valid PRF bit is set.

	D7	D6	D5	D4	D3	D2	D1	D0
$0508	CHANNEL MODE		CHANNEL BLOCK		NON VALID PRF	PRF VALUE		

Bit	Function
7 to 4	same as section 5.1.2.1, bits 3 to 0
3	Non Valid PRF 0 - valid PRF 1 - incomplete PRF data block
2 to 0	PRF value 000 - 0.5 KHz 001 - 1 KHz 010 - 2 KHz 011 - 5 KHz 100 - 10 KHz 101 - 15 KHz 110 - 20 KHz 111 - 25 KHz

5.1.5.4 Spare Register ($0509)

This byte is reserved for future applications.

5.1.5.5 Event Word ($050A and $050B)

The 16-bit Event Word is used to load event codes into the header for a particular PRF data block. Each time a new event occurs in the system, a code is stored in the header. This code corresponds to an event stored in the acquisition session file.

These bits come from the MTU and are read from the 16-bit parallel port. This is a read only word.

	D7	D6	D5	D4	D3	D2	D1	D0
$050A	D15	D14	D13	D12	D11	D10	D9	D8
$050B	D7	D6	D5	D4	D3	D2	D1	D0

5.1.6 Spare Register ($050C)

This byte is reserved for future applications.

5.1.7 Diagnostics ($050D to $051F)

This group of registers monitors the activity on the DCIB from the DCS Controller Card. Two registers are read only words which monitor the data at the DFB interface and the DSP interface. A third register reads the address counter value. The fourth register is used to replace the sample data words coming from the High Speed Bus by simulated data. A status register is also provided to monitor the status of the header FIFO buffer.

5.1.7.1 Diagnostic Status Register ($050D)

The Diagnostics Status register enables the on-board diagnostics and allows the DCS Controller Card to simulate sample data at the input. Also, this register provides status of the header FIFO.

	D7	D6	D5	D4	D3	D2	D1	D0
$050D	HEADER FIFO FULL	HEADER FIFO EMPTY	X	X	DIAG ENABLE	X	X	X

Bit	Function
7	Header FIFO full 0 - not full 1 - full
6	Header FIFO empty 0 - not empty 1 - empty
3	Diagnostics enable 0 - disabled 1 - enabled

5.1.7.2 DFB Data Word ($050E and $050F)

The 16-bit DFB Data Word being sent to the DFB can be read at addresses $050E and $050F. This is a read only word.

	D7	D6	D5	D4	D3	D2	D1	D0
$050E	D15	D14	D13	D12	D11	D10	D9	D8
$050F	D7	D6	D5	D4	D3	D2	D1	D0

5.1.7.3 DSP Data Word ($0510 to $0513)

The 32-bit DSP Data Word being sent to the DSP interface can be read at addresses $0510 to $0513. This is a read only word.

	D7	D6	D5	D4	D3	D2	D1	D0
$0510	D31	D30	D29	D28	D27	D26	D25	D24
$0511	D23	D22	D21	D20	D19	D18	D17	D16
$0512	D15	D14	D13	D12	D11	D10	D9	D8
$0513	D7	D6	D5	D4	D3	D2	D1	D0

5.1.7.4 Data Block Address Counter ($0514 to $0517)

The 21-bit Data Block Address Counter is available at addresses $0514 to $0517. This is a read only word

	D7	D6	D5	D4	D3	D2	D1	D0
$0514	X	X	X	X	X	X	X	X
$0515	X	X	X	D20	D19	D18	D17	D16
$0516	D15	D14	D13	D12	D11	D10	D9	D8
$0517	D7	D6	D5	D4	D3	D2	D1	D0

5.1.7.5 Sample Data Bus Data ($0518 to $051F)

The 48-bit High Speed Bus Data can be simulated via these registers. When the diagnostic bit in the Diagnostics Status Register is set, the sample data source comes from these registers instead of the high speed bus.

	D7	D6	D5	D4	D3	D2	D1	D0
Upper High Speed Bus, A								
$0518	X	X	X	X	D11	D10	D9	D8
$0519	D7	D6	D5	D4	D3	D2	D1	D0
Lower High Speed Bus, A								
$051A	X	X	X	X	D11	D10	D9	D8
$051B	D7	D6	D5	D4	D3	D2	D1	D0
Upper High Speed Bus, B								
$051C	X	X	X	X	D11	D10	D9	D8
$051D	D7	D6	D5	D4	D3	D2	D1	D0
Lower High Speed Bus, B								
$051E	X	X	X	X	D11	D10	D9	D8
$051F	D7	D6	D5	D4	D3	D2	D1	D0

6. REFERENCES

[1] *Development of an Enhanced Signal Processing Data Acquisition and Display System*, MultiDev JDL Communications Inc., June 1995.
[2] *Differential Fast Bus Interface Manual*, revision 2.0, Storage Concepts, May 1989.
[3] *IXI32D Manual: 32-Bit High speed Differential Interface*, revision 1.0, Ixthos, June 1995.
[4] *EARS High Speed Analog to Digital Converter Unit - Interface board Detailed Design*, Applied Silicon, August 1994.

APPENDIX A: CONNECTORS PIN-OUT

1. Differential Fast Bus
2. Upper High Speed Bus & Low Speed Bus (J1)
3. Lower High Speed Bus (J2)
4. Digital Signal Processing Bus
5. Transmit Frequency Interface

DIFFERENTIAL FAST BUS

1-	GND
3-	RSTB+
5-	IORDY+
7-	WSTB+
9-	P16_LO+
11-	DB00+
13-	DB01+
15-	DB02+
17-	DB03+
19-	DB04+
21-	DB05+
23-	DB06+
25-	DB07+
27-	DB08+
29-	DB09+
31-	DB10+
33-	DB11+
35-	DB12+
37-	DB13+
39-	DB14+
41-	DB15+
43-	MRDY+
45-	P16_HI+
47-	BLOCK+
49-	N. C.

2-	N. C.
4-	RSTB-
6-	IORDY-
8-	WSTB-
10-	P16_LO-
12-	DB00-
14-	DB01-
16-	DB02-
18-	DB03-
20-	DB04-
22-	DB05-
24-	DB06-
26-	DB07-
28-	DB08-
30-	DB09-
32-	DB10-
34-	DB11-
36-	DB12-
38-	DB13-
40-	DB14-
42-	DB15-
44-	MRDY-
46-	P16_HI-
48-	BLOCK-
50-	GND

UPPER HIGH SPEED BUS & LOW SPEED BUS (J1)

PIN	ROW A	ROW B	ROW C
1	CHSDAU0	LSC0	CHSDBU0
2	CHSDAU1	CHSCS0	CHSDBU1
3	CHSDAU2	CHSCS1	CHSDBU2
4	CHSDAU3	N. C.	CHSDBU3
5	CHSDAU4	GND	CHSDBU4
6	CHSDAU5	N. C.	CHSDBU5
7	CHSDAU6	N. C.	CHSDBU6
8	CHSDAU7	PRF+	CHSDBU7
9	GND	PRF-	GND
10	CHSCLKU	20MHz+	CHSDBU8
11	GND	20MHz-	CHSDBU9
12	CHSDAU8	CLSA8	CHSDBU10
13	CHSDAU9	CLSA7	N. C.
14	CHSDAU10	CLSA6	N. C.
15	GND	CLSA5	N. C.
16	CHSDAU11	CLSA4	N. C.
17	GND	CLSA3	N. C.
18	CHSDBU11	CLSA2	CHSA20
19	GND	CLSA1	CHSA19
20	LSC1	GND	CHSA18
21	IRQ	CLSA0	CHSA17
22	RESET	CLSD7	CHSA16
23	CHSA7	GND	CHSA15
24	CHSA6	CLSD6	CHSA14
25	CHSA5	CLSD5	CHSA13
26	CHSA4	CLSD4	CHSA12
27	CHSA3	CLSD3	CHSA11
28	CHSA2	CLSD2	CHSA10
29	CHSA1	CLSD1	CHSA9
30	CHSA0	CLSD0	CHSA8
31	N. C.	N. C.	N. C.
32	+5V	+5V	+5V

LOWER HIGH SPEED BUS (J2)

PIN	ROW A	ROW B	ROW C
1	CHSDAL0	N. C.	CHSDBL0
2	CHSDAL1	CHSCS0	CHSDBL1
3	CHSDAL2	CHSCS1	CHSDBL2
4	CHSDAL3	N. C.	CHSDBL3
5	CHSDAL4	N. C.	CHSDBL4
6	CHSDAL5	N. C.	CHSDBL5
7	CHSDAL6	N. C.	CHSDBL6
8	CHSDAL7	N. C.	CHSDBL7
9	GND	N. C.	GND
10	CHSCLKL	N. C.	CHSDBL8
11	GND	N. C.	CHSDBL9
12	CHSDAL8	N. C.	CHSDBL10
13	CHSDAL9	N. C.	N. C.
14	CHSDAL10	N. C.	N. C.
15	GND	N. C.	N. C.
16	CHSDAL11	N. C.	N. C.
17	GND	N. C.	N. C.
18	CHSDBL11	N. C.	CHSA20
19	GND	N. C.	CHSA19
20	N. C.	GND	CHSA18
21	N. C.	N. C.	CHSA17
22	N. C.	N. C.	CHSA16
23	CHSA7	GND	CHSA15
24	CHSA6	N. C.	CHSA14
25	CHSA5	N. C.	CHSA13
26	CHSA4	N. C.	CHSA12
27	CHSA3	N. C.	CHSA11
28	CHSA2	N. C.	CHSA10
29	CHSA1	N. C.	CHSA9
30	CHSA0	N. C.	CHSA8
31	N. C.	N. C.	N. C.
32	+5V	+5V	+5V

DIGITAL SIGNAL PROCESSING BUS

1-	D0-	2-	D0+
3-	D1-	4-	D1+
5-	D2-	6-	D2+
7-	D3-	8-	D3+
9-	D4-	10-	D4+
11-	D5-	12-	D5+
13-	D6-	14-	D6+
15-	D7-	16-	D7+
17-	D8-	18-	D8+
19-	D9-	20-	D9+
21-	D10-	22-	D10+
23-	D11-	24-	D11+
25-	D12-	26-	D12+
27-	D13-	28-	D13+
29-	D14-	30-	D14+
31-	D15-	32-	D15+
33-	D16-	34-	D16+
35-	D17-	36-	D17+
37-	D18-	38-	D18+
39-	D19-	40-	D19+
41-	D20-	42-	D20+
43-	D21-	44-	D21+
45-	D22-	46-	D22+
47-	D23-	48-	D23+
49-	D24-	50-	D24+
51-	D25-	52-	D25+
53-	D26-	54-	D26+
55-	D27-	56-	D27+
57-	D28-	58-	D28+
59-	D29-	60-	D29+
61-	D30-	62-	D30+
63-	D31-	64-	D31+
65-	DIR-	66-	DIR+
67-	ADDR0-	68-	ADDR0+
69-	ADDR1-	70-	ADDR1+
71-	DRDY-	72-	DRDY+
73-	ATTN-	74-	ATTN+
75-	STBS-	76-	STBS+
77-	THR-	78-	THR+
79-	STB-	80-	STB+

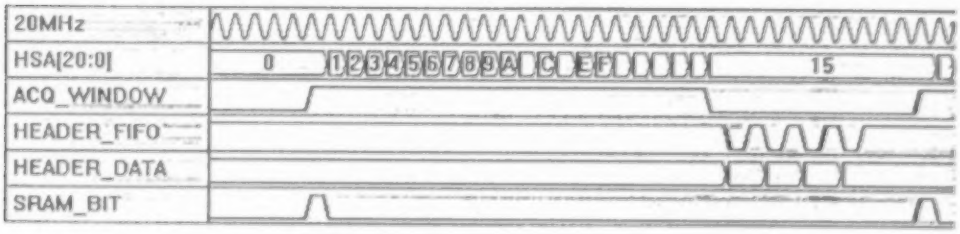
EVENT WORD INTERFACE

1-	GND
3-	D0
5-	D2
7-	D4
9-	D6
11-	GND
13-	D8
15-	D10
17-	D12
19-	D14
21-	GND
23-	CTL0
25-	CTL2

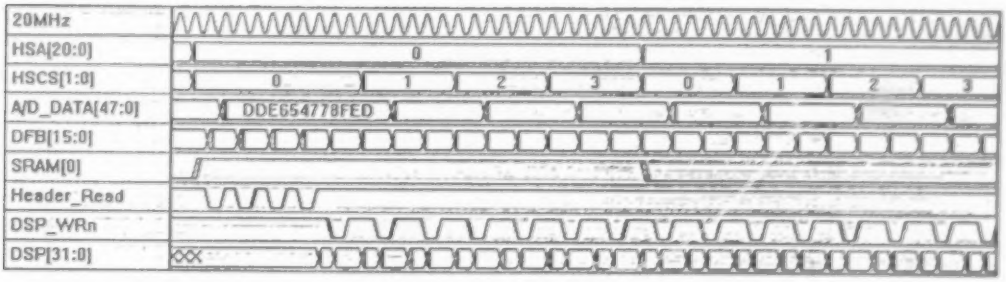
2-	GND
4-	D1
6-	D3
8-	D5
10-	D7
12-	GND
14-	D9
16-	D11
18-	D13
20-	D15
22-	GND
24-	CTL1
26-	CTL3

APPENDIX B: TIMING DIAGRAMS

DATA ACQUISITION



DATA TRANSFERS



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Data Conversion Interface Board - Detailed Design Document (U)

4. AUTHORS (Last name, first name, middle initial)

Da Sylva, Pierre
Caseault, Jean

5. DATE OF PUBLICATION (month and year of publication of document)

May 1996

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4

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Technical Report, Design Document

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Defence Research Establishment Ottawa, Radar Division
3701 Carling Ave., Ottawa, Ontario

9a. PROJECT OR GRANT NO. (if appropriate, the applicable research and development project or grant number under which the document was written. Please specify whether project or grant.)

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The EARS architecture allows the transfer of massive amount of information between the data sources and the storage subsystems. It is also capable of monitoring the transfer activity, set up the radar system for operation and control, and perform some data processing on the radar data.

The Data Conversion Interface Board is designed to allow transfers between 16 data acquisition boards (12-bit data streams) and a disk array and/or a Real-Time DSP Card. Three modes of operations are supported. In the first mode, the interface card reads data from 4, 8 or 16 AtoD Boards and transfers the data to the disk array. In the second mode of operation, the interface card reads data from 2, 4, 8 or 16 channels and transfers the data to the DSP card. The third mode is the combination of modes 1 and 2: data is sent to both the DSP card and the disk array.

The data transfer mechanism is executed in two phases. During phase one, the system acquires the data from all 16 channels and temporarily stores the data inside the AtoD Board memory buffers. When the memory buffers are full, the DCIB stops the data acquisition process and transfers the data (in groups of 4, 8 or 16 channels) to the disk array and/or to the DSP Board. During phase two, the information is transferred until the memory buffers are empty.

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EARS, Experimental Array Radar System
DATA ACQUISITION
REAL TIME PROCESSING
ANALOG TO DIGITAL CONVERSION
DATA FORMATTING
VERY LARGE DATA STORAGE
VMEBUS
OPERATING SYSTEM (OS-9)
SYSTEM DIAGNOSTICS
CONCEPT 51 DISK ARRAY
SYSTEM CONTROLLER
DIGITAL SIGNAL PROCESSING
DATA TRANSFERS

#509874